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REMARKS/ARGUMENTS

Applicants would like to thank the examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe and claim the subject matter which applicants regard as the invention.

Claims 1-29 remain in this application. Claims 30-32 are added without adding any new matter or raising any new issues.

Applicant notes that claim 20 has not been discussed by the Examiner. Thus, applicant does not know whether claim 20 has been allowed or is rejected. However, claim 20 should be allowable for the reasons discussed below.

Claims 1, 3-15, 19, and 21-30 were rejected under 35 USC 103(a) as being unpatentable over Olarig *et al.* (U.S. 6,587,909) in view of Ihara *et al.* (U.S. 6,212,580). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Olarig in view of Iharea, and further in view of Shah et al. (U.S. 6,141,711). These rejections are respectfully traversed.

Claim 1 is directed to a "data acquisition module" for a "modular data acquisition system" with the module having "at least one clock generating circuit capable of supplying an internal clock signal". The cited references do not teach these limitations of claim 1.

First, Olarig does not pertain to a data acquisition module, nor a data acquisition system. Instead, Olarig is directed toward hot-swappable memory modules for expanding the memory capability of a general purpose computer (see abstract and background). One skilled in the art would know that such memory modules are not "data acquisition modules" as they do not acquire data; instead, they merely store or retrieve data for use by the computer.

Further, there is no teaching that the memory module of Olarig has a clock generating circuit for generating an internal clock signal. The Examiner cites col. 8 line 65 to col. 9 line 35 as teaching a clock generating circuit. However, the cited

passage is discussing the features of FIG. 2, which shows circuitry located on the computer side of the memory module. Thus, the reference may teach that the *computer* has a clock circuit, but that does not teach the limitation as claimed, which is that the *module itself* has a clock generating circuit. Accordingly, the reference teaches only an *external* clock signal, and hence the reference does not teach this limitation of the claim.

In addition, claim 1 recites a "a clock selecting circuit" which "allows the selection of either a slave-clock state, in which said converters are synchronized by said synchronization bus, or of a master-clock state in which these converters are synchronized by said internal clock signal that is also used as external synchronization signal on said synchronization bus". This, also, is not suggested by the references.

The Examiner cites Olarig col 9, line 65 to col. 10, line 30; col. 3, lines 20-55; and col. 6, line 28 to col. 7, line 16 as teaching the cited passage. However, a close reading of the cited portions does not support the Examiner's assertion.

First, the "clock selecting circuit" as limited by the claim must select either the master clock state (using the internal clock signal, which, as argued above, is not taught by the reference), or a slave-clock state from the synchronization bus (e.g., using an external clock signal). The cited passages do not teach such a concept. For example, col. 10, lines 12-18 merely discuss connecting and disconnecting an *external* (i.e., off the memory module) clock signal from the slot connectors. Further, col. 3, lines 20-55 merely discuss the installation/removal of the memory module. Finally, col. 6, line 28 to col. 7, line 16, discuss functions on the computer side of the memory module. There is no suggestion of the clock selection function, and even if there was, the reference does not teach that such a function is accomplished by the module. Thus, the reference does not suggest the cited claim limitations.

Further, it is clear that the cited claim language r quires that there be *two* clock signal sources from which to choose, one that is internal, and one that is not. None of the reference suggest two such clock signals.

Finally, claim 1 recites that the module has "connecting means for removably inserting said module in a slot of the data acquisition system" and "one connector, different from said connecting means, makes it possible to plug in a removable connecting element on a second external side of said module different from the first side in order to connect said module to a synchronization bus connecting several modules in said system, said connection being effected independently from the insertion of said module into said slot". The cited references do not suggest these claim limitations.

Accordingly, the data acquisition modules of the present invention, according to the above claim language, have at least *two* connectors, one for connecting to the data acquisition device, and a second connector, placed on *another* side of the module (e.g., on the front side), for connecting to a synchronization bus. The references do not suggest these claim limitations.

The Examiner cites Olarig at col. 3, lines 20-55 and col. 6 line 27 to col. 7, line 16, as teaching the above claim limitations. However, neither passage suggests two connectors. Column 3, lines 20-55 discusses an operation that isolates the memory module connectors to allow hot-swapable memory removal, but does not suggest two connectors on a memory module. Likewise, col. 6 line 27 to col. 7 discuss only a single slot connector. Hence, the reference does not suggest two connectors as required by the claim language.

Consequently, as discussed above, the Olarig reference fails to teach a number of the claim limitations. None of the additionally cited references overcome the above discussed shortcomings of Olarig. Accordingly, claim 1 is patentable over the references, whether taken individually or in any combination. Claims 2-29, which depend, directly or indirectly, on claim 1, are thus patentable over the

references for at least the same reasons. New claims 30 and 31 are each patentable over the references for one or more of the reasons discussed above, as is claim 32, which is dependent on claim 31.

Further, with respect to the alleged obviousness over Olarig in view of Ihara, neither the references themselves nor some other prior art suggest that they be combined. The mere mention that ADC may be used to convert an analog signal made by Salo can not constitute an incitation to combine these two references. "To reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made [and] the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person." (MPEP §2142, emphasis added). It is not proper to merely combine various elements from various references without providing the proper motivation for doing so. The invention must be obvious "as a whole", not piecemeal, and the motivation must be from the prior art; merely providingthe benefits of the disputed features is not a proper motivation. Thus, the rejection for obviousness is improper, and should be withdrawn.

Claims 16-18 were rejected under 35 USC 103(a) as being unpatentable over Olarig in view of Iharea, and further in view applicants admitted prior art (AAPA). for the following reasons, the rejection is respectfully traversed:

The Examiner argues that applicant has admitted that it is know to utilize acquisition modules to conform to the PCI, CompactPCI, VXI, or PXI standards. Even if true, applicant notes that the Examiner has merely provided hindsight motivation, i.e., motivation from the application itself, for adding the features of claims 16-18 to the cited references. This is clearly improper, as the facts must be gleaned from the prior art. (MPEP §2142, last paragraph). Accordingly, the rejection is improper and should be withdrawn.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 33307.

Respectfully submitted,

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May 6, 2004